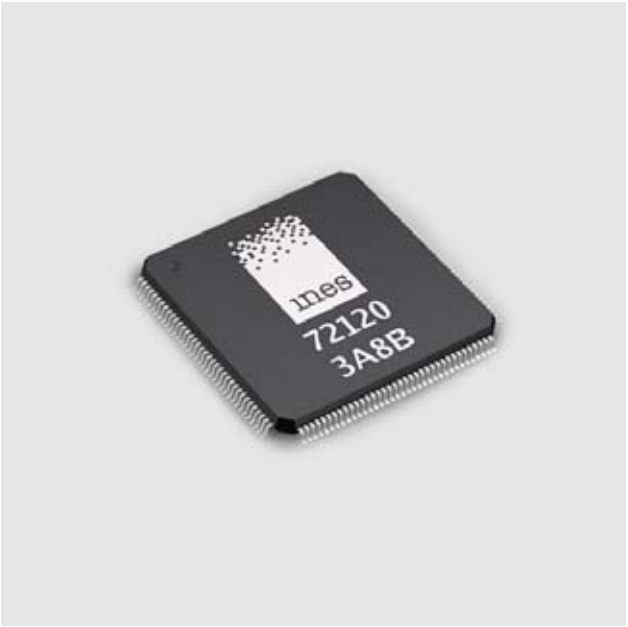
i72120

PCI to GPIB interface ASIC



Features

- **Talker/Listener interface for instrumentation devices**
- **PCI v2.2 32-bit/33MHz Target with 3.3 VCC, 3.3/5.0 VIO**
- **NEC µPD7210 compatible register layout**
- **144 pin TQFP package**
- **RoHS conformant (Pb-free)**

Description

The i72120 GPIB-Chip is the ideal solution to implement a IEEE488.2 GPIB interface for next generation PCI based instruments. The GPIB-ASIC is designed to meet all of the functional requirements for talker and listener (TL) devices as specified by the IEEE Standards 488.1-1987 and 488.2-1987. Connected between the PCI bus and the GPIB, this GPIB-IC provides high-level management of the GPIB to unburden the processor and to simplify both hardware and software design. The i72120 is fully compatible with the PCI specification and requires only the addition of bus driver/receiver components to implement a talker/listener GPIB interface.

History

The IEEE Standard 488 describes a "Standard Digital Interface for Programmable Instrumentation" which, since its introduction in 1975 has become the most popular means of interconnecting instruments and controllers in laboratory, automatic test, and even industrial applications. Refined over several years, the 488-1978 Standard, also known as The General Purpose Interface Bus (GPIB), is a highly sophisticated standard providing a high degree of of flexibility to meet virtually all instrumentation requirements. The i72120 implements all of the functions that are required to interface to the GPIB as a talker or listener device. While it is beyond of the scope of this document to provide a complete explanation of the IEEE 488 Standard, a basic descriprion follows:

The GPIB interconnects up to 15 devices over a commom set of data control liners. Three types of devices are defined by the standard: talker, listener, and controller, atthough some devices may combine functions such as talker/listener or talker/controller.

Data on the GPIB is transferred in a bit-parallel, byte-serial fashion over eight data I/O lines (/DIO[1]-/DIO[8]). A three-wire handshake is used to ensure synchronisation of transmission and reception. In order to permit more than one device to receive data at the same time, these control lines are "open collector" so that the slowest device controls the data rate. A number of other control lines perform a variety of functions such as device addressing, interrupt generation and so forth.

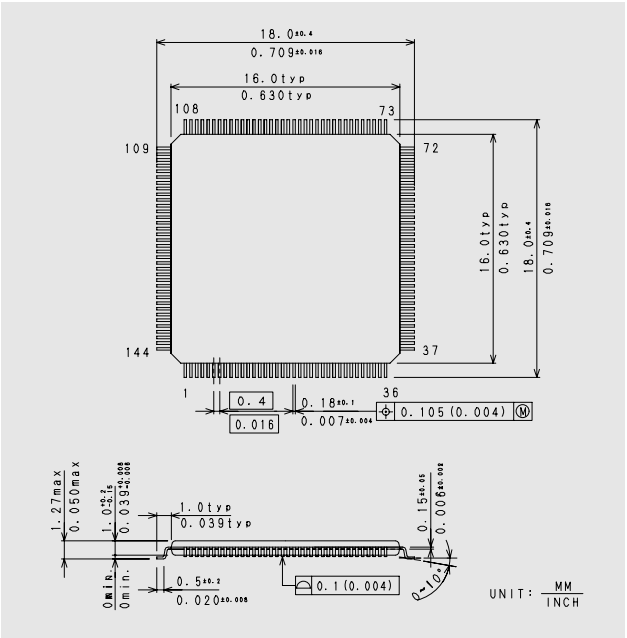
The i72120 implements all functional aspects of talker and listener as defined by the 488.1-1987 Standard on a single chip.

Pin Functions

Pinout

Pin	Function	Type	Pin	Function	Type
1	NDACoen	OUTPUT	2	NRFDoen	OUTPUT
3	RENo	OUTPUT	4	PCI_RSTNi	INPUT
5	NC	NC	6	SRQoen	OUTPUT
7	VCC	VCC	8	ATNi	INPUT
9	DAVi	INPUT	10	EOIi	INPUT
11	IFCi	INPUT	12	SRQi	INPUT
13	RENi	INPUT	14	NRFDi	INPUT
15	GND	GND	16	NDACi	INPUT
17	PDN	PDN	18	PDN	PDN
19	VCC	VCC	20	RSTN	INPUT
21	CLK	INPUT	22	VCC	VCC
23	INTAon	OUTPUT	24	AD[31]	BIDIR
25	AD[30]	BIDIR	26	AD[29]	BIDIR
27	AD[28]	BIDIR	28	AD[27]	BIDIR
29	AD[26]	BIDIR	30	CND	GND

Pin	Function	Type	Pin	Function	Type
31	AD[25]	BIDIR	32	AD[24]	BIDIR
33	CBEN[3]	INPUT	34	IDSEL	INPUT
35	AD[23]	BIDIR	36	AD[22]	BIDIR
37	AD[21]	BIDIR	38	PUP	PUP
39	AD[20]	BIDIR	40	AD[19]	BIDIR
41	AD[18]	BIDIR	42	VCC	VCC
43	AD[17]	BIDIR	44	AD[16]	BIDIR
45	CBEN[2]	INPUT	46	FRAMEN	INPUT
47	IRDYN	INPUT	48	TRDYN	BIDIR
49	DEVSELN	BIDIR	50	GND	GND
51	STOPN	BIDIR	52	PERRN	BIDIR
53	SERRN	BIDIR	54	GND	GND
55	PAR	BIDIR	56	CBEN[1]	INPUT
57	AD[15]	BIDIR	58	VCCIO	VCCIO
59	AD[14]	BIDIR	60	AD[13]	BIDIR
61	AD[12]	BIDIR	62	AD[11]	BIDIR
63	AD[10]	BIDIR	64	AD[9]	BIDIR
65	AD[8]	BIDIR	66	GND	GND
67	CBEN[0]	INPUT	68	AD[7]	BIDIR
69	AD[6]	BIDIR	70	AD[5]	BIDIR
71	LOW	INPUT	72	HIGH	INPUT
73	AD[4]	BIDIR	74	AD[3]	BIDIR
75	AD[2]	BIDIR	76	AD[1]	BIDIR
77	AD[0]	BIDIR	78	PDN	INPUT
79	VCC		80	NC	BIDIR
81	PDN	INPUT	82	NC	BIDIR
83	NC	BIDIR	84	NC	BIDIR
85	NC	BIDIR	86	NC	BIDIR
87	GND	GND	88	NC	BIDIR
89	PDN	CLKPAD	90	PDN	CLKPAD
91	VCC	VCC	92	PDN	CLKPAD
93	PDN	CLKPAD	94	VCC	VCC
95	NC	BIDIR	96	NC	OUTPUT
97	NC	OUTPUT	98	NC	OUTPUT
99	NC	OUTPUT	100	PDN	INPUT
101	PDN	INPUT	102	GND	GND
103	NC	OUTPUT	104	DIOi[1]	INPUT
105	DIOi[2]	INPUT	106	DIOi[3]	INPUT
107	DIOi[4]	INPUT	108	DIOi[5]	INPUT
109	LOW109	INPUT	110	LOW110	INPUT
111	DIOi[6]	INPUT	112	DIOi[7]	INPUT
113	DIOi[8]	INPUT	114	VCC	VCC
115	DIOo[1]	OUTPUT	116	DIOoen[1]	OUTPUT
117	DIOo[2]	OUTPUT	118	DIOoen[2]	OUTPUT
119	DIOo[3]	OUTPUT	120	DIOoen[3]	OUTPUT
121	DIOo[4]	OUTPUT	122	GND	GND
123	DIOoen[4]	OUTPUT	124	DIOo[5]	OUTPUT
125	DIOoen[5]	OUTPUT	126	GND	
127	DIOo[6]	OUTPUT	128	DIOoen[6]	OUTPUT
129	DIOo[7]	OUTPUT	130	VCCIO	VCCIO
131	DIOoen[7]	OUTPUT	132	DIOo[8]	OUTPUT
133	DIOoen[8]	OUTPUT	134	ATNo	OUTPUT
135	ATNoen	OUTPUT	136	DAVo	OUTPUT
137	DAVoen	OUTPUT	138	GND	GND
139	EOIo	OUTPUT	140	EOIoen	OUTPUT
141	IFCo	OUTPUT	142	IFC_RENoen	OUTPUT
143	NC		144	LOW144	INPUT



Specifications

GPIB Capabilities

IEEE 488.1 Capabilities: AH1, SH1, T/TE5, L/LE3, SR1, RL1, PP1/PP2, DC1, DT1, C0
GPIB Handshake Rate: > 1Mbytes/sec

Environmental and Physical

Package: 144 TQFP, 22.0 mm x 22.0 mm x 1.6 mm
Storage Temperature: -20…80°C
Ambient Temperature: -0…70°C

Ordering Information

i72120-33 - Tray of 60 units

On the Web

Click www.inesinc.com for more information and resources.

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