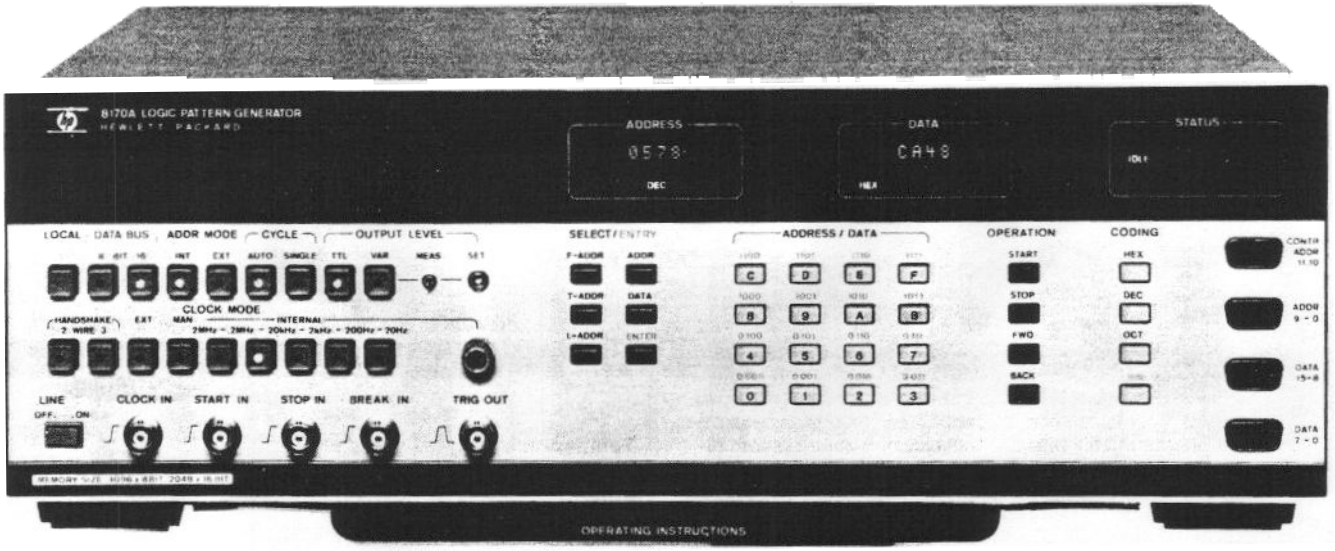
PULSE & DATA GENERATORS

Logic pattern generator for bus stimulation

Model 8170A

- 8 k memory (32 k option)
- 8 bit / 16 bit parallel output
- 2 wire / 3 wire handshake capability
- Internal and external addressing



DESIGNED FOR HP-IB SYSTEMS

Introduction

The 8170A Logic Pattern Generator is a real-time test stimulus for functional checkout of today's multi-channel logic devices and subassemblies. With data traffic in modern digital systems routed over a shared bus, the 8170A's direct bus driving capability makes design verification at every stage in system development and production a quick, straightforward task.

Data generation by the 8170A is in parallel 8-bit or 16-bit format, to a memory depth of 1024 or 512 words respectively (optionally extendable to four times that capacity). This, combined with a variable clock rate up to 2 MHz permits thorough functional testing at full system operating speed. In addition, output levels of the 8170A ensure a direct match to today's most widely employed logic families—TTL and CMOS, while specially designed mini-probes minimize hook-up problems to the device under test.

Selectable Codes

Designed around the 6800 microprocessor, the 8170A's control scheme permits data, address and operating modes to be entered directly via the instrument keyboard. A sophisticated feature of keyboard programming is the multi-code format available for address and data. Codes include octal, decimal and hexadecimal (see specifications), the microprocessor automatically performing code conversion to the binary base. When fast program check or recall is required, alphanumeric LED's display individual data-address lines in the selected code.

Internal Address Mode

The 8170A's internal address mode is specifically intended for driving digital busses. Typical bus traffic is simulated by generating data in an ascending address sequence, the first and last address being preset by the user. The 8170A can be thus programmed for detailed investigation of selected bus functions.

Whether the tested bus operates synchronously or asynchronously, the 8170A generates the necessary test signal. With NORM selected, the 8170A outputs data in response to a clock signal (internal, external or manual). Where a bus operates in an asynchronous 2-wire or 3-wire handshake system, the 8170A generates data and data valid signals in accordance with the selected protocol.

External Address Mode

In external address mode, 8170A operation is analogous to the RE-PROM. Data is output according to the state of externally applied address and enable lines. The main advantage using the 8170A is the ease with which data can be loaded or modified via the keyboard—as opposed to generally complicated processes demanded by RE-PROM's. Where time is a valuable commodity such as in software test and development, the 8170A presents significant savings in this mode.

HP-IB

With full programmability via the HP-IB interface bus, the 8170A's application base extends to automated test systems. Employing microprocessor control over all interface functions, a syntax has been developed to make remote programming of the 8170A as simple as manual operation.

RS 232C-CCITT V.24

In many applications, a multi-line readout is necessary for quick program set-ups and checks. For this reason, the 8170A is designed to be compatible with the serial RS 232C/CCITT V.24 interface standard. By linking the 8170A to a low cost data terminal over this interface, the multi-line listing of the 8170A memory enables fast data modification.

Specifications

Memory Size
Capacity: 8 kbit.
Data bus format: 8 bit or 16 bit wide.

Operating States
Idle: permits entry of address, data and operating parameters.
Active: continuous data output.
Break: pause in data output. FWD/BACK enables further data output.

Address Modes
Internal: data generation in ascending address sequence from F-ADDR to L-ADDR (F-ADDR, L-ADDR = user-defined first and last addresses).
External: data output follows external address and enable signals. DAV generated at each new address. Data and DAV high impedance when instrument not enabled. Clock and cycle modes disabled.
Maximum address rate: 2 MHz.
Address to output delay: 400 ns typ., 550 ns max.
Enable to output delay: 100 ns typ., 130 ns max. DAV at min.delay.

Clocking
Internal: 20 Hz to 2 MHz in 5 decade ranges.
Rate jitter: <0.2%
External: dc to 2 MHz. For inp. specs, see "Auxiliary inputs".
Manual: operated by FWD and BACK key.
Handshake: 2-wire/3-wire handshake capability selectable.

Cycle Modes
Auto cycle: data is continuously generated between F- and L-ADDR.
Single cycle: data is generated once between F- and L-ADDR. After cycle completion, 8170A returns to IDLE state.

Output Signals
Data: pods provide 16 output lines D0-D7 (model 15455A), low byte, and D8-D15 (model 15456A), high byte. Pos./neg. true select on rear panel.
Control: data valid (DAV) generated with each word. Pos./neg. true selectable on rear panel.
DAV delay (adjustable on rear panel)
Non-handshake: 100 ns to 700 ns.
2- or 3-wire handshake: 300 ns to 800 ns.
Status: idle, active and break states indicated on lines ACS and BRS.

Pod Output Levels
TTL setting
Fan out: 5 standard TTL max.
Levels: high +4.5 V to +5 V; low −0.5 V to +0.4 V; idle 6 mA to ground.
Transition times (+0.4 V to +2.4 V): 25 ns typ. 50 ns max.
Variable setting
Maximum load: 50 pF (high impedance)
Levels: high +3 V to +15 V adj., low −0.5 V to +0.4 V.
Transition times (20% to 80%): 35 ns typ. 60 ns max.

Auxiliary Outputs
Trigger: generated at trigger address (T-ADDR).
Format: NRZ.
Levels: standard TTL.
Fan out: 5 standard TTL.
Probe: +5 V dc.
Address driver outputs (Opt. 002): provides 10 address output lines A0 to A9, positive true.
Fan out: 10 standard TTL.
Levels: high +2.4 V; low +0.5 V; idle 1.5 mA to +5 V.
Transition times (+0.5 V to +2.4 V): 50 ns.

Pod Input Signals
Input RC: >10 kΩ/≤25 pF.
Levels: high ≥+2.0 V; low ≤+0.8 V.
Max. external voltage: ±18 V.
Address input pod (Model 15453A): 10 addressable input lines A0-A9 for operation in external address mode.
Control input pod (Model 15454A): following inp. lines available:
Ready for data (RFD), data accepted (DAC): for handshake mode. In 2-wire handshake RFD level selectable pos./neg. true. In 3-wire handshake, fixed levels for RFD, DAC (see IEE Std. 488-1975)
Enable E1, E2 (E3, E4 at rear panel): for operation in ext. address mode. Selectable levels pos./neg./don't care.
Address A10, A11: for extended memory, option 001.

Auxiliary Inputs
Clock in: for external clock signal input.
Start in: external signal starts data generation. Prompts 8170A transition from idle/break to active state.
Stop in: external signal stops data generation. Prompts 8170A transition from active/break state to idle state.
Break in: external signal halts 8170A at current address, outputs remain active. Prompts 8170A transition from active to break state.
Input conditions (all positive edge triggered)
Input RC: >10 kΩ/≤25 pF.
Levels: high ≥+2.0 V, low ≤+0.8 V.
Min. width (at +1.3 V): Clock 40 ns; Start/Stop/Break 20 ns.
Max. external voltage: ±18 V.

HP-IB
Keyboard mode: remote programming of all front panel keys and functions. Coded loading and readout of data.
Data mode: fast binary loading and readout of data only.

RS 232C/CCITT V.24.
Remote editing and listing of memory content, and display of current data bus format and address/data coding.
Baud rate: 110, 150, 300, 600, 1200, 2400, 4800, 9600 selectable.

General
Power: 100/120/220/240 V rms; +5% − 10%; 48 - 66 Hz, 110 VA max.
Operating Temperature: 0°C to 55°C.
Weight: net 11 kg (24.3 lbs), shipping 15 kg (33.2 lbs).
Dimensions: 133 H x 426 W x 422 mm D (5.2 x 16.8 x 16.6 in).

Accessories Supplied
2 data output pods (15455A/6A), 1 address input pod (15453A), 1 control pod (15454A), a 2 m power cord and an operating/service manual. Each pod includes Snap-on Assembly 15458A for clip connection to DUT.

Ordering Information
8170A Logic Pattern Generator*
Opt 001: 32 kbit Memory
Opt 002: Address Driver Pod (Model 15452A).
Opt 907: Front Handle Kit (part number 5061-0089).
Opt 908: Rack Mount Kit (part number 5061-0077).
Opt 909: Opt 907, 908 Combined (part number 5061-0083).
Opt 910: Extra Operating and Service Manual.
15457A Pod Connector (Pods can be easily plugged into DUT when this accessory is wired in).
15263A Card Reader: rapid memory loading
*HP-IB cables not furnished, see page 30.